LISTING OF AND AMENDMENTS TO CLAIMS:

1.- 14. (canceled)

15. (currently amended) A method for forming an interconnection structure suitable for flip-chip attachment of microelectronic device chips to packages, comprising:

forming a ball limiting composition on a substrate;

forming a resist pattern on the ball limiting composition;

etching the ball limiting composition by using the resist as an etch mask;

removing the resist from remaining ball limiting composition; and

depositing a predominantly Sn lead free solder on the ball limiting composition so as to form a eutectic solder.

16. (canceled).

17. (original) A method as recited in claim 15, wherein the ball limiting composition is formed by:

depositing an adhesion layer on said substrate;

depositing a reaction barrier layer on said adhesion layer; and

depositing a solder wettable layer on said barrier layer.

18. (original) A method as recited in claim 17, wherein said reaction barrier layer is comprised of a

material selected from the group consisting of Ti, TiN, Ta, TaN, Zr, ZnN, V and Ni.

19. (original) A method as recited in claim 17, wherein said adhesion layer is deposited by sputtering, plating or evaporating.

20. (original) A method as recited in claim 17, wherein said adhesion layer is deposited so as to have a thickness of about 100 to about 4000 Angstroms.

21. (original) A method as recited in claim 17, wherein said reaction barrier layer is deposited by sputtering, plating or evaporation.

22. (original) A method as recited in claim 21, wherein said reaction barrier layer is deposited so as to have a thickness of about 100 to about 20,000 angstroms.

23. (original) A method as recited in claim 17, wherein said solder wettable layer is deposited by sputtering, plating or evaporation.

24. (original) A method as recited in claim 17, wherein said solder wettable layer is deposited so as to have a thickness of about 100 to about 20,000 angstroms.

25. (original) A method as recited in claim 17, further comprising depositing a layer comprising Au or Sn on said solder wettable layer.

26. (original) A method as recited in claim 25, wherein the layer deposited on said solder wettable layer has a thickness of between substantially 100 to substantially 20,000 angstroms.

27. (original) A method as recited in claim 25, wherein the layer deposited on said solder wettable layer is deposited by one of sputtering, electro- or electroless plating or evaporation.

28. (canceled)

29. (original) A method as recited in claim 15, further comprising annealing the ball limiting composition at 150 - 250 degrees C for 30 to 60 minutes.

30. (currently amended) A method for forming an interconnection structure suitable for flip-chip attachment of microelectronic device chips to chip carriers, comprising:

depositing an adhesion layer on a wafer or substrate serving as said chip carrier;

depositing a solder reaction barrier layer on said adhesion layer;

depositing a solder wettable layer on said reaction barrier layer, said solder wettable layer containing Cu;

depositing a lead free solder on said solder wettable layer, said lead free solder being substantially binary Sn-Ag; and

reflowing said solder so that said solder wettable layer diffuses into said lead free solder;

wherein said Cu of said solder wettable layer diffuses into said solder, and a ternary Sn-Ag-Cu lead-free solder is formed during reflowing.

31. (canceled).

32. (canceled).

33. (canceled).

34. (currently amended) A method as recited in claim 30 [[33]], wherein a eutectic solder is formed.

35. A method as recited in claim 30, wherein a number of elements in said solder is increased by at least one element, by said diffusion.

36. A method as recited in claim 30, further comprising annealing at 150 - 250 degrees C for 30 to 60 minutes.

37. - 46. (canceled).

47. (new) A method as recited in claim 15, wherein the predominantly Sn lead free solder contains greater than 90 % by weight Sn.

48. (new) A method as recited in claim 15, wherein the predominantly Sn lead free solder contains one or more alloying components selected from the group consisting of Cu, Zn, Ag, Bi and Sb, whereby the lead-free solder

substantially avoids alpha particle emission and induced soft logic errors which result therefrom.

49. (new) A method as recited in claim 17, wherein the solder wettable layer comprises Cu.

50. (new) A method as recited in claim 49, wherein the solder wettable layer is a Cu layer having a thickness of 1-6 microns.

51. (new) A method for forming an interconnection structure suitable for flip-chip attachment of microelectronic device chips to chip carriers, comprising:

depositing an adhesion layer on a wafer or substrate serving as said chip carrier;

depositing a solder reaction barrier layer on said adhesion layer;

depositing a solder wettable layer on said reaction barrier layer, said solder wettable layer containing Cu;

depositing a lead free solder on said solder wettable layer, said lead free solder being substantially pure Sn; and

reflowing said solder so that said solder wettable layer diffuses into said lead free solder;

wherein said Cu of said solder wettable layer diffuses into said solder, and a binary Sn-Cu eutectic lead-free solder is formed during reflowing.